v^1 Concept: Designing a Voltage-Mode Control as Current Mode With Near Time-Optimal Response for Buck-Type Converters

Jorge Cortés, Vladimir Šviković, Pedro Alou, Jesús A. Oliver, and José A. Cobos

***Abstract*—This paper introduces the v^1 concept that explains how by only measuring the output voltage, designers have information about almost every signal of the power stage. Following the v^1 concept, it is explained how to design a traditional type-III voltage-mode control to behave like a current-mode control with near time-optimal response under load transients. This study is validated in simulations and experimentally on a 300-kHz buck converter.**

***Index Terms*—Buck, capacitor current, current mode, optimal, POL, *v*1, *v*2, *v*2ic, voltage mode.**

I. Introduction

APPLICATIONS with highly demanding load steps and dynamic voltage scaling such as point-of-load converters and voltage regulator modules need very fast controls in order to comply with the dynamic requirement and still maintain an output capacitor as small as possible.

Ripple-based controls are one popular solution to achieve a fast dynamic response. They are composed by a fast feedback (FFB) path and a slow feedback (SFB) path. The FFB path is a rippled signal with information about the power stage, and it is responsible of the modulation of the duty cycle and the dynamic behavior of the control. The SFB path is an integrator designed to have a very low bandwidth and it is responsible to regulate the output voltage in steady state.

The v^2 control [1], [2] only uses the output voltage, but it behaves properly only with high-ESR output capacitors [3]. In [4] and [5], the inductor current is added to the v^2 control to stabilize it. On the other hand, Del Viejo *et al.* [6] proposed in 2011, instead, to add the capacitor current information using only the output voltage, which allows the control to behave almost optimally under load transients [7], [8]. This control is named $v^2 i_c$ (or "current-mode control of the output capacitor current" in a previous version from 2010 [9]). Using the capacitor current to improve the dynamic response is not a new concept since it dates back at least to 1986 [10], but [6] improves the idea by using a simple lossless sensor of the capacitor that only measures the output voltage and that takes into account the ESL of the output capacitor. In 2013, Yan *et al.* [11] proposed the same concept with a different implementation of the sensor of the current. Later in 2014, Google filed a patent including the same concept as in [9] but with a different sensor of the capacitor current [12].

Another approach for fast dynamic response are the minimum time controls [13]–[20], which precalculate the control action to achieve a time-optimal response or a near-optimal response with current limit. These controls are digitally implemented and behave in open loop during transient responses so their correct behavior is not guaranteed under pulsating loads.

Also, adaptive controls [21]–[29] are a trending topic in the area of improving the dynamic response of converter. These controls change parameters of the control (ramp, hysteretic band, etc) according to the conditions of the system. This approach can improve the robustness of the control and/or its dynamic response compared to its nonadaptive counterpart. Yet, this advantage comes at the expense of a more complex control system.

As seen, in the scientific literature, a wide variety of controls appear to provide a fast dynamic response. However, from the point of view of the industry, low-cost simple solutions to control the converter are needed.

This paper shows how by only measuring the output voltage and just with a type-III controller, an extremely fast reaction under load steps can be achieved, if designed correctly. This paper is structured as follows. Section II reviews the fundamental behavior of ripple-based controls and proposed control topologies. Section III introduces the v^1 concept and shows the basic idea on how to design the voltage-mode controls. Section IV explains with examples for different output capacitors how to design the voltage-mode control and its possible implementations. Section V explains the difference between traditional designs of voltage-mode control and the proposed designs and proposes a design flow to implement the control. Section VI shows the experimental validation of the proposed methodology and Section VII summarizes the contributions of this paper. The simulation results of this paper are obtained from the program Simplis.

II. Review of Ripple-Based Controls

The v^2 control is the most popular ripple-based control (see Fig. 1) [1], [2]. In v^2 control, the rippled signal of the FFB path is the output voltage [see Fig. 1(a)]. In the case where the output

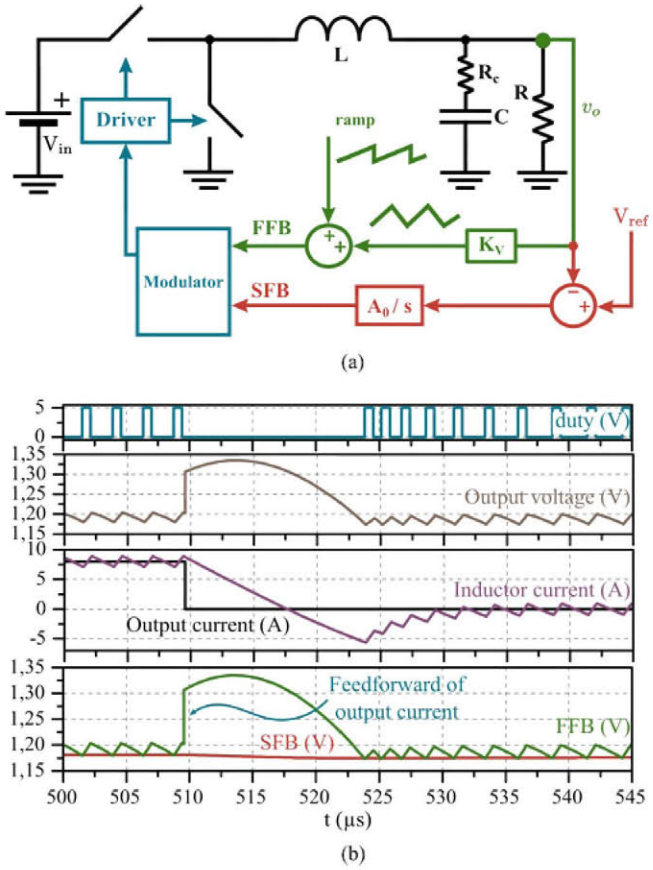

Fig. 1. v^2 control of a buck converter. (a) General scheme of a v^2 control on a buck converter. (b) Load transient response for v^2 with constant on-time modulation.

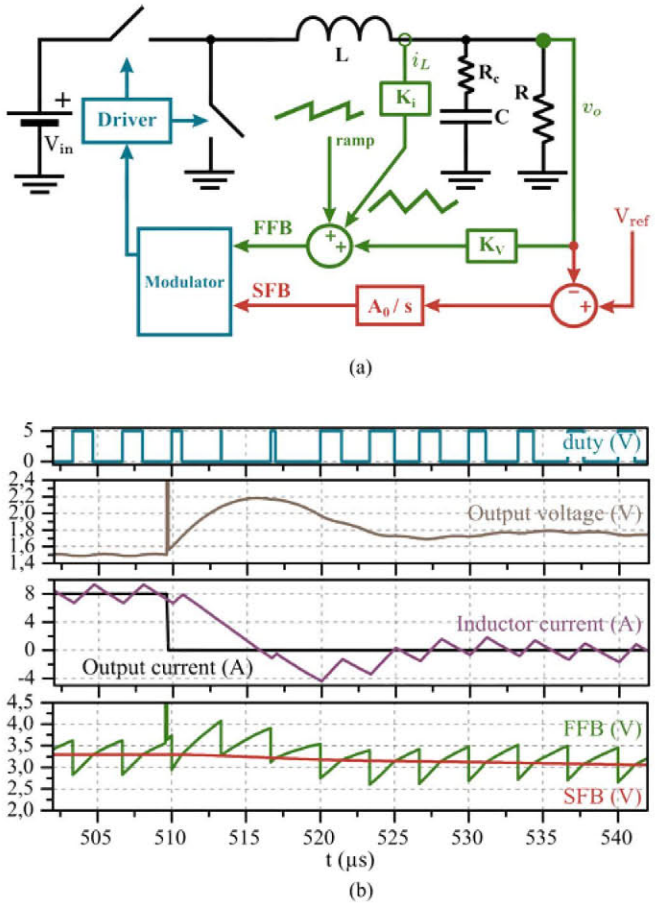

Fig. 2. $v^2 i_L$ control of a Buck converter. (a) General scheme of a $v^2 i_L$ control of a buck converter. (b) Load transient response for $v^2 i_L$ with constant frequency modulation.

capacitor has dominant ESR, the output voltage ripple provides information about the capacitor current, which has combined information of the inductor current and the output current. Consequently, the output voltage is shaped as the inductor current and can be used to modulate the duty cycle as in current-mode control, while exhibiting fast dynamic response due to an inherent feedforward of the output current [see Fig. 1(b)].

Note that the v^2 control only uses the output voltage but behaves like a current-mode control when the ESR of the output capacitor is large.

For low ESR capacitors such as ceramic capacitors, the current information in the ripple of the output voltage is not dominant and, therefore, an additional current ripple has to be added. A popular way in the industry is to add directly the inductor current to the rippled signal (see Fig. 2), usually sensed with an *R–C* network. Then, the FFB path is composed by the sum of the output voltage and the inductor current [see Fig. 2(a)]. This control is proposed under the name of enhanced-v^2 control [4] and it is also named v^2 control with current injection [5] but in this paper, we will call it $v^2 i_L$ for simplicity. As the information of the output current is limited for low ESR capacitors, this control achieves a suboptimal load transient response under these operating conditions [see Fig. 2(b)].

Instead of adding the inductor current, a better approach is to add the capacitor current (see Fig. 3). Then, the FFB path is composed by the sum of the output voltage and the capacitor current [see Fig. 3(a)]. This control is named $v^2 i_c$ [6] and it was later proposed in [11] and [12] with different implementations but the same concept. As the capacitor current provides the control with information about the output current, $v^2 i_c$ reacts under load transient almost optimally even for low ESR capacitors [3] [see Fig. 3(b)]. The dynamic response can be further improved by synchronizing the modulator with the load step [8].

For the implementation of $v^2 i_c$, the capacitor current can be sensed by using only the output voltage by designing a transimpedance amplifier with an impedance proportional to the impedance of the real-output capacitor, including the ESR and the ESL [30]. Fig. 4 shows a scheme of the implementation of $v^2 i_c$, where $K_i/Z_c(s)$ represents the sensor of the capacitor current. Note that, as with v^2 control with high-ESR capacitors, $v^2 i_c$ behaves like a current-mode control, but only senses the output voltage.

III. v^1 Concept: Designing a Voltage-Mode Control that Behaves Like a Current-Mode Control

Even if ripple-based controls only sense the output voltage (v^2 and $v^2 i_c$), they are in nature current-mode controls. This is because the output voltage has inherently information of the

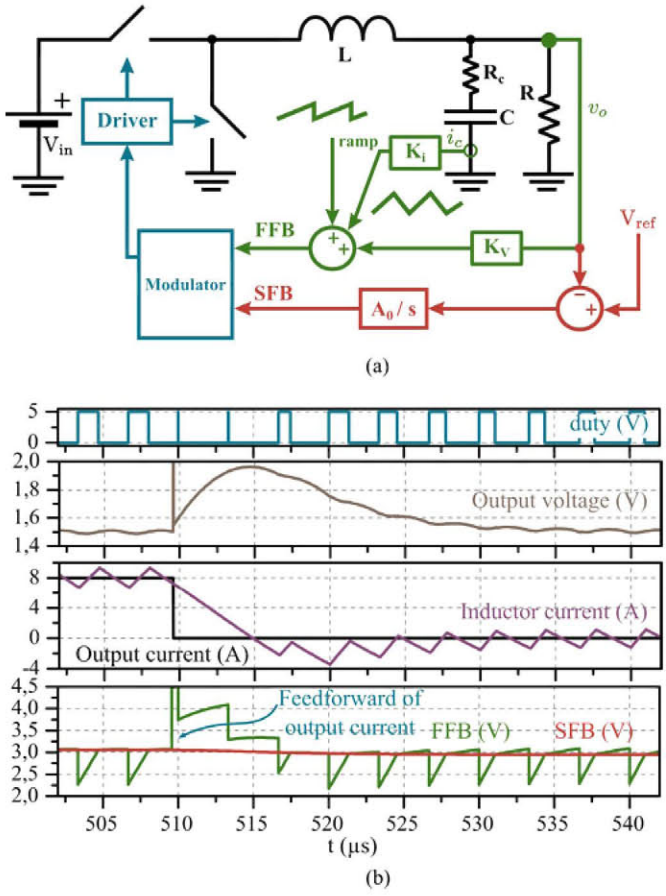

Fig. 3. $v^2 i_c$ control of a buck converter. (a) General scheme of a $v^2 i_c$ control of a buck converter. (b) Load transient response for $v^2 i_c$ with constant frequency modulation.

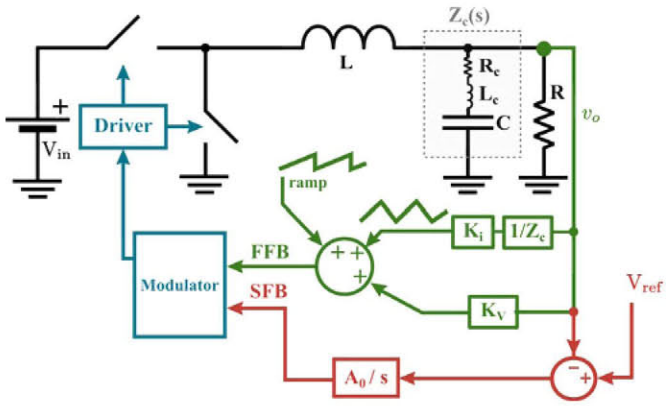

Fig. 4. Scheme of $v^2 i_c$ sensing the capacitor current using only the output voltage. This sensor of the capacitor current is explained in [30].

capacitor current (from the ESR of the capacitor or by using a transimpedance amplifier). Also, the capacitor current itself has combined information of the inductor current and the output current. This information about the output current is very important because it is what allows the v^2 and $v^2 i_c$ controls to behave almost time optimally under a load transient. Additionally, the inductor current has information of the input voltage during the

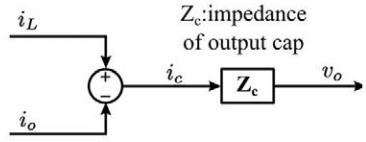

Fig. 5. v^1 concept. The output voltage has information about almost all the signals of the power stage.

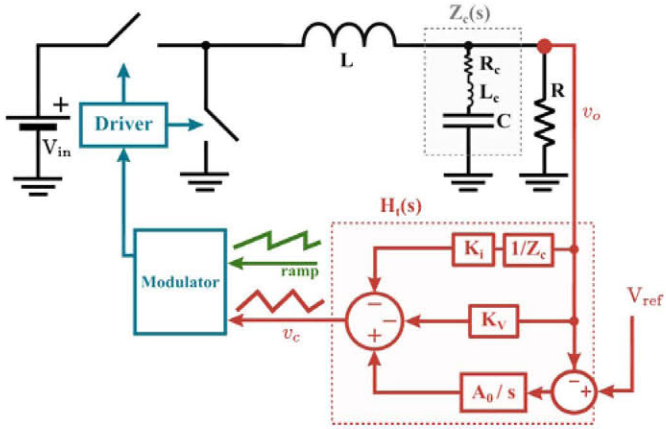

Fig. 6. Alternative representation of $v^2 i_c$ control.

on-time. This concept of only sensing once the output voltage and using its inherent information about the power stage is what we call v^1 (see Fig. 5).

Following the v^1 concept, the question then arises whether a traditional voltage-mode control can be designed in a way so that this intrinsic information is exploited and, consequently, it behaves like a current-mode control with a very fast dynamic response. This voltage-mode control could be modulated, as ripple-based and current-mode controls, with constant frequency (peak or valley), constant on-time, constant off-time, or hysteretic modulations.

Fig. 4 shows the structure of the $v^2 i_c$ control where the capacitor current is sensed with a transimpedance amplifier with an impedance proportional to the impedance of the output capacitor and implemented with two paths, the SFB and the FFB path. Now, as an alternative equivalent representation, both the sensing of the capacitor current and the output voltage of the FFB path can be deducted to the output of the integrator (see Fig. 6).

The equivalent regulator $H_t(s)$ is

$$H_t(s) = \frac{A_0}{s} + K_v + K_i \frac{1}{Z_c(s)} \tag{1}$$

where

$$Z_c(s) = \frac{L_c C s^2 + R_c C s + 1}{Cs}. \tag{2}$$

Fig. 7 shows the Bode diagram of the controller of (1). This regulator has an integral action, A_0/s, which regulates tightly the output voltage, a proportional action K_v, that provides a zero to the regulator, boosting the phase, and a weighted estimator of the capacitor current, $K_i/Z_c(s)$ that converts voltage

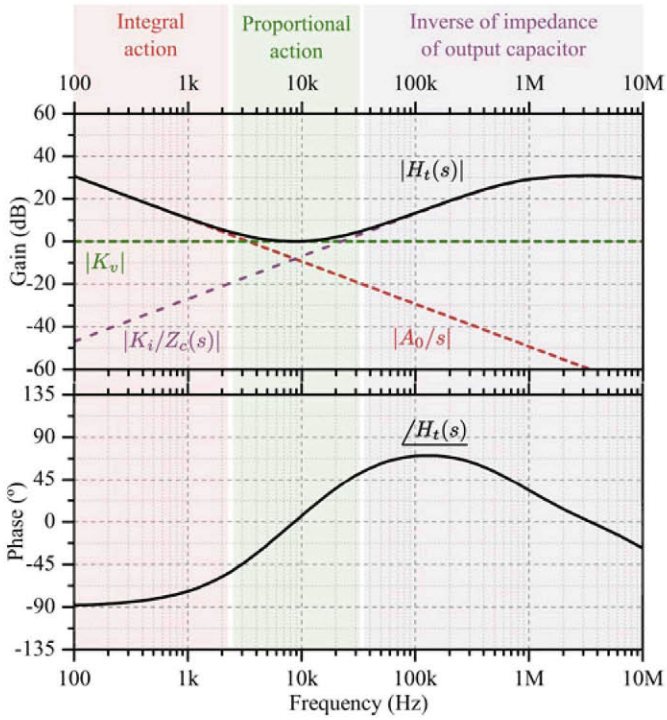

Fig. 7. Decomposition of the frequency response of the equivalent regulator of $v^2 i_c$ $H_i(s)$.

information into current information. As shown in Section II, this current sensor is very important because it provides the control a feedforward of the output current, needed to obtain a near time-optimal response under load transients.

Equation (1) and Fig. 7 are very important because they synthesize the objective of this paper, in order to obtain a voltage-mode control that behaves like a current mode with near time-optimal response under load transients, the regulator needs to mirror the impedance of the output capacitor at high frequencies. Of course, it is important to comment that a perfect matching of the impedance of the output capacitor is not possible in an actual product. Tolerances of the output capacitor due to aging, temperature and dc bias will have to be considered when designing the controller. Its effect on the stability can be studied and the control can be optimized by means of the procedure proposed in [31] and [32], respectively.

Now the fundamental question is: is it possible to use the information about the capacitor current with a traditional voltage-mode control?

IV. Implementable Designs of Voltage-Mode Control for Different Output Capacitors

The answer to the previous question is that it depends on the specific impedance of the output capacitor. This section provides the design guidelines for different types of output capacitor.

Equation (2) showed the impedance of the output capacitor and it can be rewritten as

$$Z_c(s) = \frac{1 + \frac{\sqrt{L_c C}}{Q} s + L_c C s^2}{Cs} \tag{3}$$

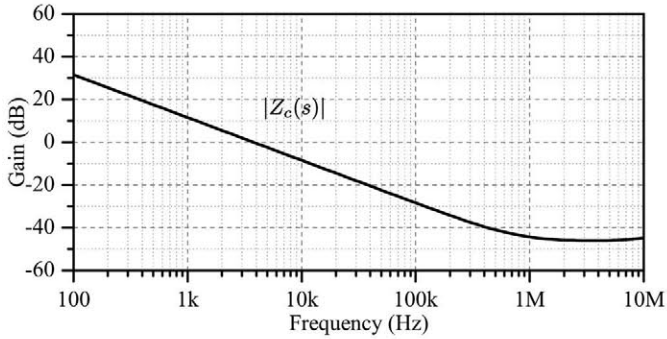

Fig. 8. Impedance of a low-Q capacitor ($C = 42$ μF, $R_c = 5$ mΩ, $L_c = 50$ pH). The impedance has two real zeros.

where Q is the quality factor

$$Q = \frac{\sqrt{L_c/C}}{R_c}. \tag{4}$$

The quality factor, Q establishes whether $Z_c(s)$ has real or complex zeros. If $Q < 0.5$, then the impedance of the output capacitor exhibits real zeros. If $Q > 0.5$, then the impedance of the output capacitor exhibits complex zeros.

A. Low-Q Output Capacitor

For output capacitor with low quality factor ($Q < 0.5$), the zeros of the impedance of the capacitor are real. Therefore, the impedance of the output capacitor can be approximated as

$$Z_c(s) = \frac{\left(1 + sCR_c\right)\left(1 + s\frac{L_c}{R_c}\right)}{Cs}. \tag{5}$$

Fig. 8 shows the Bode diagram of a capacitor with this behavior ($C = 42$ μF, $R_c = 5$ mΩ, $L_c = 50$ pH).

From (1) and (5), the equivalent regulator, $H_t(s)$, can be found out graphically. Fig. 9 shows the Bode diagram of the proposed design of the equivalent regulator for the case of a low-Q output capacitor. The controller has then a zero z_1 located at the intersection between the integral and the proportional part, another zero, z_2, located at the intersection between the proportional part and the inverse of $Z_c(s)$ and, then, the poles of the inverse of $Z_c(s)$. As a result, the equivalent regulator $H_t(s)$ is

$$H_t(s) = A_0 \frac{\left(1 + \frac{s}{z_1}\right)\left(1 + \frac{s}{z_2}\right)}{s\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)} \tag{6}$$

where

$$z_1 = \frac{A_0}{K_v}, \quad z_2 = \frac{K_v}{K_i C}, \quad p_1 = \frac{1}{CR_c}, \quad p_2 = \frac{R_c}{L_c}. \tag{7}$$

This regulator is a traditional type-III voltage-mode control (see Fig. 10). Note that the design of the type-III controller places a pole at the zero of the ESR of the output capacitor. This is a common design guideline given by manufacturers [33].

For the simulation results, the power stage has the following parameters: $V_{\text{in}} = 5$ V, $v_o = 1.5$ V, $L = 1.5$ μH, $C = 42$ μF,

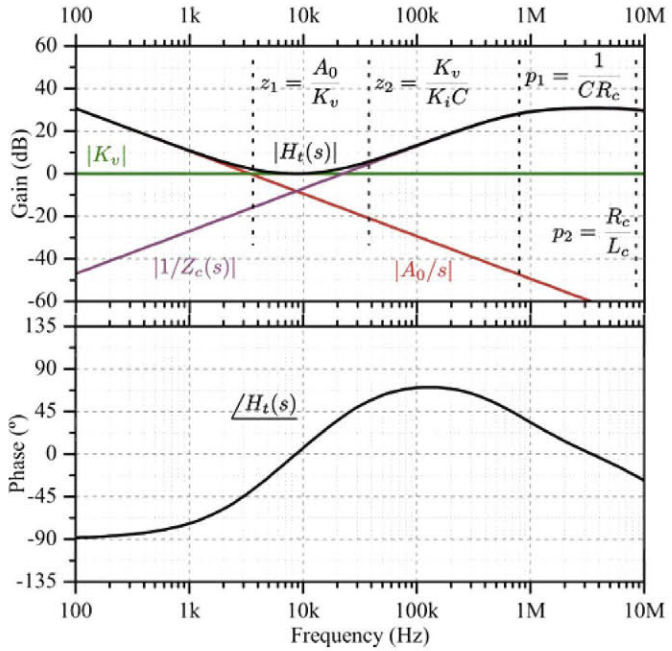

Fig. 9. Proposed design of the regulator for low-Q output capacitors. Notice that it is a type-III controller.

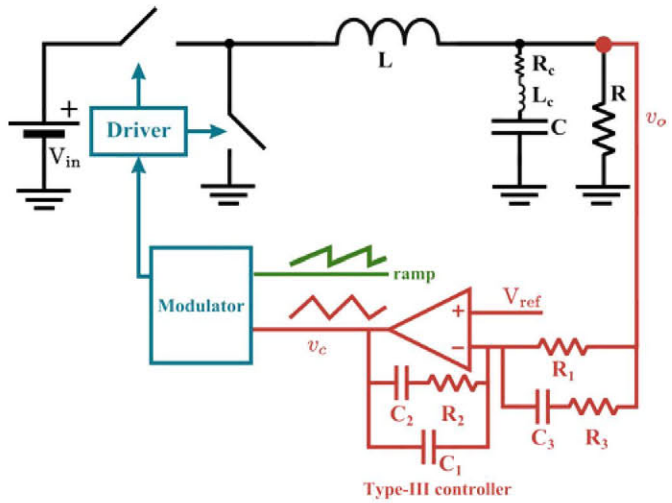

Fig. 10. Scheme of a type-III voltage-mode control.

$R_c = 5\ \text{m}\Omega$, $L_c = 50\ \text{pH}$, $f_{\text{sw}} = 300\ \text{kHz}$. The control parameters are $K_v = 1$, $K_i = 0.17$, $A_0 = 21.28\ \text{k}$. The amplitude of the compensating ramp is $0.8\,\text{V}$. The resulting exact passive elements of the type-III controller are (see Fig. 10), $R_1 = 1\ \text{k}\Omega$, $R_2 = 193.44\ \Omega$, $R_3 = 5.27\ \Omega$, $C_1 = 54.48\ \text{pF}$, $C_2 = 46.95\ \text{nF}$, $C_3 = 37.93\ \text{nF}$. Of course, in a real implementation of the controller, the values of the passives would be rounded to the nearest standard value.

Fig. 11 shows the large-signal behavior of the type-III voltage-mode control. Fig. 11(a) shows the steady-state behavior of the signals of the comparator v_c and the ramp, and Fig. 11(b) shows the response under a load step. Note that the designed type-III voltage-mode control achieves a near time-optimal response and

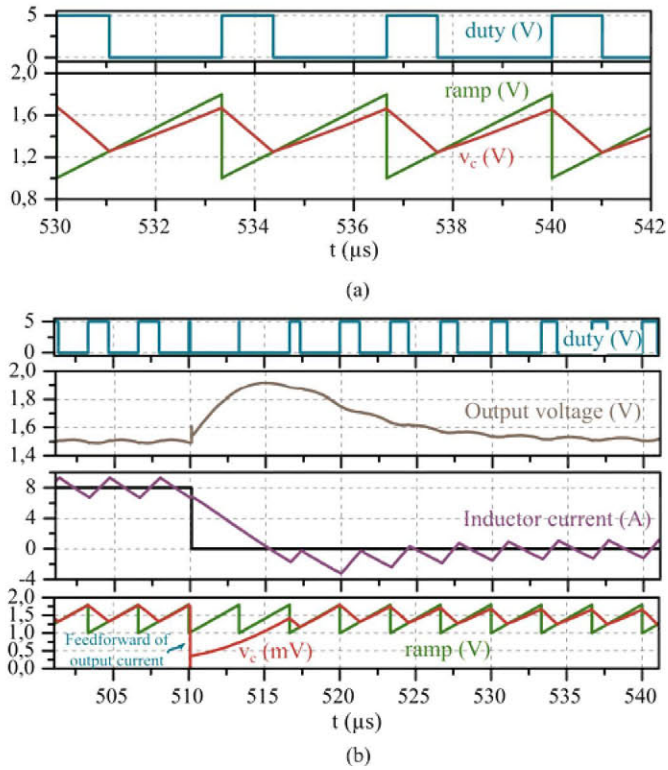

Fig. 11. Large-signal behavior of proposed design of type-III voltage-mode control with constant frequency modulation for a low-Qoutput capacitor. (a) Steady-state signals of the comparator. (b) Load transient response 8 A → 0 A.

exhibits a feedforward of the output current. Consequently, it has been shown that with a correct placement of poles and zeros of a type-III compensator, a traditional voltage-mode control can exhibit a feedforward of the output current. Also note that this control is equivalent to the $v^2 i_c$ control of Fig. 3(b), that has the same parameters A_0, K_v, and K_i and achieves the exactly same transient response. Additionally, as for this type of capacitor, the $v^2 i_c$ control and the designed type-III voltage-mode control are equivalent, their robustness under changes of the output capacitor due to tolerances are also the same. Also note that as this designed voltage mode is behaving like a current mode, it can be modulated with constant on-time or hysteretic modulation.

B. High-Q Output Capacitor

For high-Q capacitors ($Q > 0.5$), the capacitance and the ESL of the output capacitor resonate and create two conjugate complex poles. Therefore, the impedance of the output capacitor can be rewritten as

$$Z_c(s) = \frac{1 + \frac{1}{Q w_c} s + \frac{1}{w_c^2} s^2}{Cs} \tag{8}$$

where w_c is the resonant frequency

$$w_c = \frac{1}{\sqrt{L_c C}} \tag{9}$$

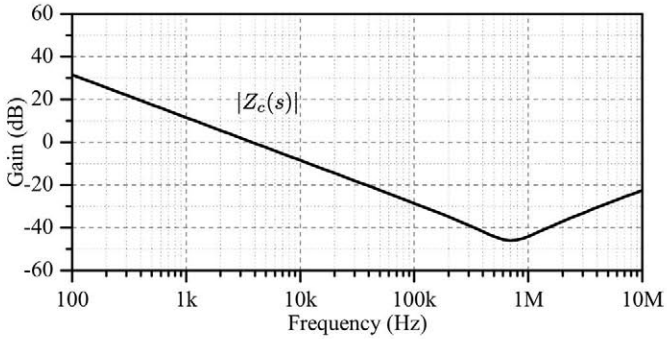

Fig. 12. Impedance of a high-Q output capacitor, where C and ESL resonate ($C = 42\ \mu$F, $R_c = 5$ mΩ, $L_c = 1.2$ nH). The impedance has conjugate complex zeros.

and Q is the quality factor

$$Q = \frac{\sqrt{L_c/C}}{R_c}. \tag{10}$$

Fig. 12 shows the Bode diagram of a capacitor with this behavior ($C = 42\mu$ F, $R_c = 5$ mΩ, $L_c = 1.2$ nH).

Using the same approach as for the case of low-Q output capacitor, the equivalent regulator $H_t(s)$ is

$$H_t(s) = A_0 \frac{\left(1+\frac{s}{z_1}\right)\left(1+\frac{s}{z_2}\right)}{s\left(1+\frac{1}{Qw_c}s+\frac{1}{w_c^2}s^2\right)} \tag{11}$$

where

$$z_1 = \frac{A_0}{K_v}, \quad z_2 = \frac{K_v}{K_i C}. \tag{12}$$

As the regulator has complex poles, the exact (11) can be implemented only as a $v^2 i_c$ control. This is a very important feature of $v^2 i_c$ control because the phase variation of the complex poles has a larger slope compared to real poles. This means that the complex poles have less effect at frequencies below the resonant frequency compared to real poles, which start decreasing the phase from approximately one decade below of the pole frequency. Consequently, a large phase margin can be achieved more easily.

However, an approximated version of the regulator can be implemented as a type-III voltage mode by placing the real poles at the same frequency as the complex poles

$$H_t(s) \approx A_0 \frac{\left(1+\frac{s}{z_1}\right)\left(1+\frac{s}{z_2}\right)}{s\left(1+\frac{1}{w_c}s\right)^2}. \tag{13}$$

This approximation is only valid if the bandwidth of the control is at least one decade lower than the resonance frequency of the output capacitor w_c.

Fig. 13 shows the equivalent compensator of $v^2 i_c$ control modulated with constant switching frequency for a specific case. The power stage has the following parameters: $V_{\text{in}} = 5$ V, $v_o = 1.5$ V, $L = 1.5\ \mu$H, $C = 42\ \mu$F, $R_c = 5$ mΩ, $L_c = 1.2$ nH, $f_{\text{sw}} = 300$ kHz. The control parameters of $v^2 i_c$ are:

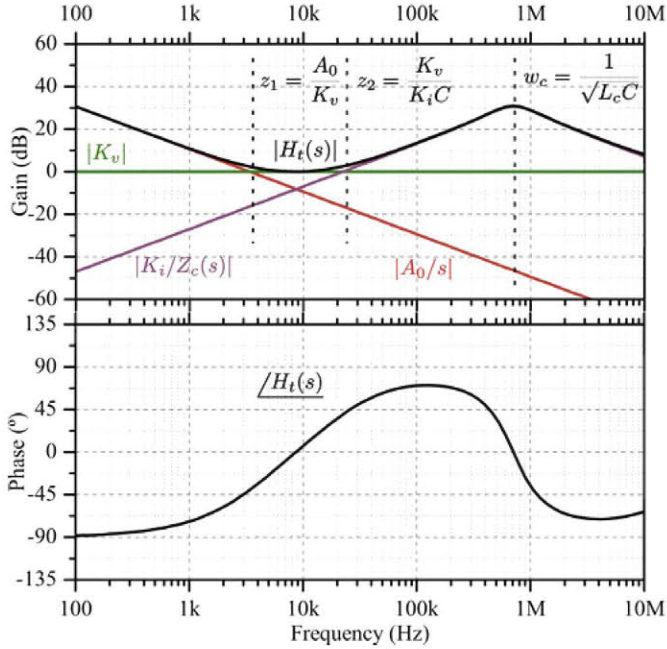

Fig. 13. Equivalent regulator of (1) and $v^2 i_c$ control for the case of a high-Q output capacitor.

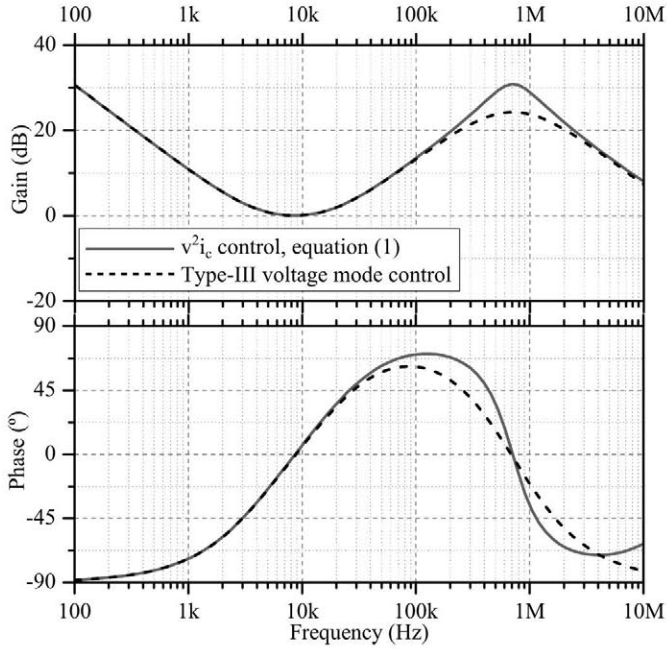

Fig. 14. Comparison between equivalent regulator of $v^2 i_c$ control and proposed design of type-III regulator for the case of a high-Q output capacitor.

$K_v = 1$, $K_i = 0.17$, $A_0 = 21.28$ k. The amplitude of the compensating ramp is 0.8 V. The resulting passive elements of the type-III controller are (see Fig. 10) $R_1 = 10$ kΩ, $R_2 = 2$ kΩ, $R_3 = 60\ \Omega$, $C_1 = 117$ pF, $C_2 = 4.6$ nF, $C_3 = 3.8$ nF.

Fig. 14 compares the equivalent regulator of the $v^2 i_c$ control and the regulator of the type-III controller. Note that, as the $v^2 i_c$

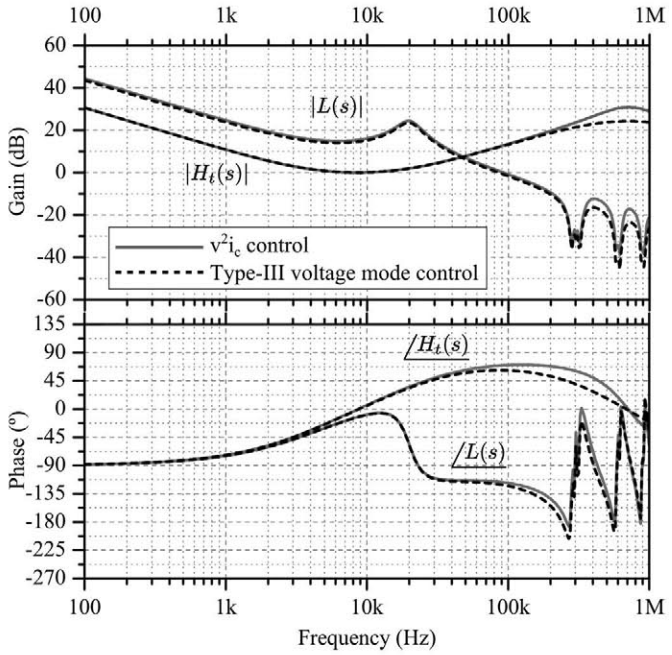

Fig. 15. Comparison between the regulators $H_t(s)$ and the loop gains $L(s)$ of $v^2 i_c$ control and proposed design of type-III voltage-mode control with constant frequency modulation.

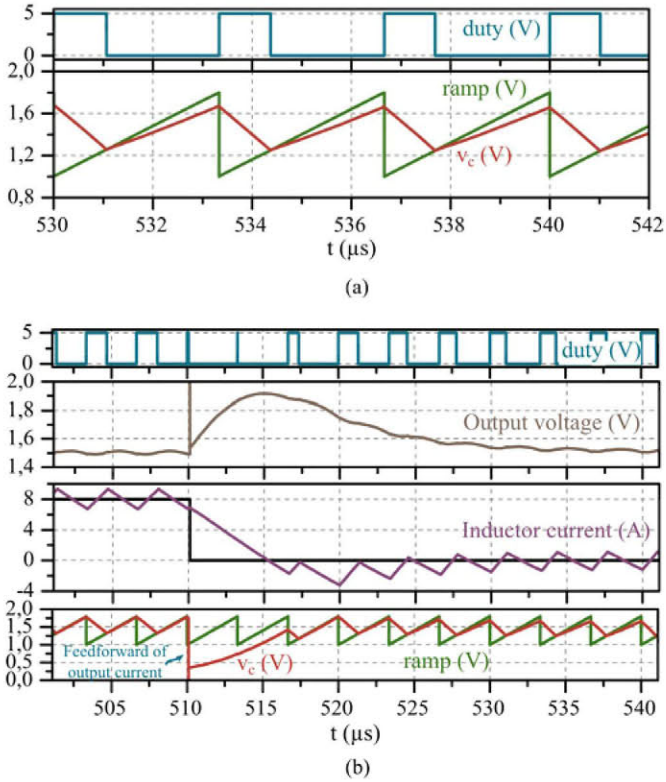

Fig. 16. Large-signal behavior of $v^2 i_c$ control with constant frequency modulation for a high-Q output capacitor. (a) Steady-state signals of the comparator. (b) Load transient response 8 A $\rightarrow$ 0 A.

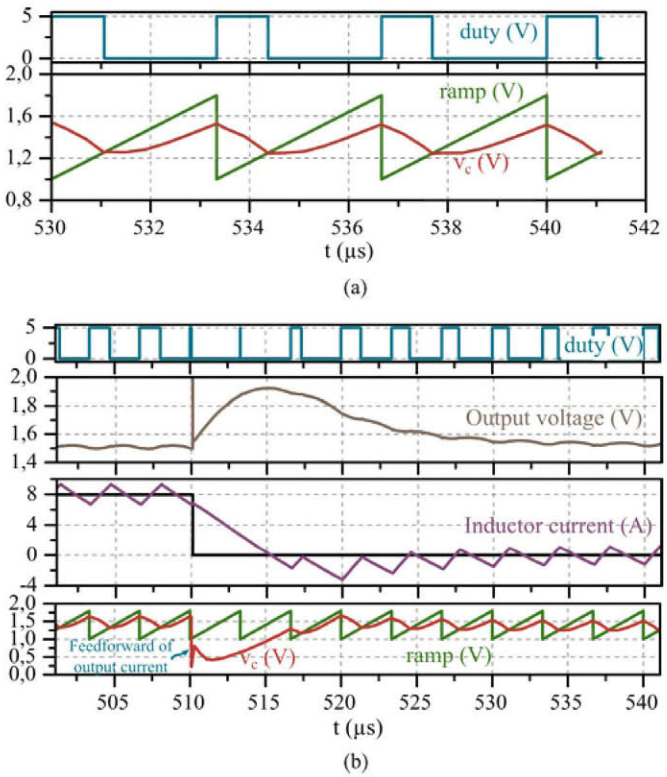

Fig. 17. Large-signal behavior of proposed design of type-III voltage-mode control with constant frequency modulation for a high-Q output capacitor. (a) Steady-state signals of the comparator. (b) Load transient response 8 A $\rightarrow$ 0 A.

control exhibits complex poles, it can achieve a larger phase boost for the same placement of the zeros.

Fig. 15 compares the regulators and the loop gains of the $v^2 i_c$ and the type-III voltage mode. Both controls exhibit almost the same loop gain. Note the difference in the phase around the poles of the voltage-mode control due to the complex poles featured by the $v^2 i_c$ control. However, as the bandwidth of the loop gain is one decade lower than the resonance frequency of the impedance of the output capacitor, the phase margin is almost the same for both designs ($\approx$60°). Figs. 16 and 17 show the large-signal behavior of the $v^2 i_c$ and the type-III voltage-mode control, respectively, where the $v^2 i_c$ is implemented as in Fig. 6. Fig. 16(a) shows for the $v^2 i_c$ control the steady-state behavior of the signals of the comparator v_c and the ramp, and Fig. 16(b) the response under a load step. Note that the steady state and the dynamic response is almost exactly the same as the type-III voltage-mode control of case A (see Fig. 11). This is expected as the control parameters A_0, K_v, K_i are the same and the only thing that changes is the ESL of the output capacitor.

Fig. 17(a) and (b) shows the same waveforms for the type-III voltage-mode control. Note that both controls achieve exactly the same transient response, which is near time optimal and exhibits a feedforward of the output current. Consequently, it has been shown that, for cases where the C and the ESL of the output capacitor resonates and provided that the bandwidth is at least one decade below than the resonant frequency, a type-III voltage-mode control can be designed that behaves like a current mode with near time-optimal response.

However, for cases where the bandwidth of the loop gain is close to one decade below the resonant frequency, the robustness of the implementation of (1) as a $v^2 i_c$ control is better than its

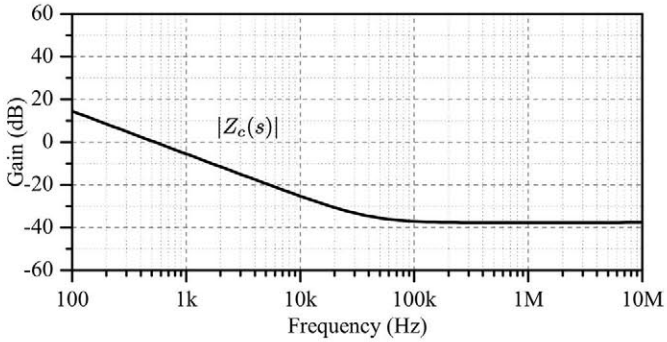

Fig. 18. Impedance of output capacitor with ESR-zero at low frequencies ($C = 300\ \mu$F, $R_c = 13\ \text{m}\Omega$, $L_c = 50$ pH). The impedance is the ESR for medium and high frequencies.

approximated implementation as a type-III voltage-mode control. This is because when the tolerances of the output capacitor increase the bandwidth of the loop gain, the phase margin of the $v^2 i_c$ does not decrease much due to the presence of complex poles, that exhibits a faster phase drop compared to real poles, that start decreasing the phase from one decade below.

C. Capacitor With ESR-Zero at Low Frequencies

A special case of a low-Q output capacitor is if the zero created by the ESR is placed at low frequencies. In these cases, for frequencies above the ESR-zero of the capacitor, the impedance of the output capacitor is equal to its ESR R_c

$$Z_c \approx R_c. \tag{14}$$

Fig. 18 shows the Bode diagram of a capacitor with this behavior ($C = 300\ \mu$F, $R_c = 13\ \text{m}\Omega$, $L_c = 50$ pH).

From (1), the equivalent regulator $H_t(s)$ is then

$$H_t(s) = A_0/s + K_v + K_i/R_c. \tag{15}$$

If (1) is implemented as a $v^2 i_c$ control, then the gain K_i is a degree of freedom. However, it is better to lose that degree of freedom for the sake of simplicity and combine K_v and K_i/R_c into a single parameter. Then, (15) is simplified as

$$H_t(s) = A_0/s + K_v = A_0 \frac{1 + \frac{s}{z_1}}{s} \tag{16}$$

where

$$z_1 = \frac{A_0}{K_v}. \tag{17}$$

This regulator is a traditional type-II voltage-mode control and it is also the equivalent regulator of the v^2 control.

Fig. 19 shows how the v^2 control is an alternative implementation of a type-II voltage-mode control. Fig. 19(a) shows the traditional structure of the v^2 control. For generality, a compensating ramp has been added into the FFB path. An equivalent representation is shown in Fig. 19(b), where the weighted output voltage of the FFB path has been instead deducted to the output of the integrator. This representation is already a traditional voltage-mode control, where the equivalent compensator is the same as (16)

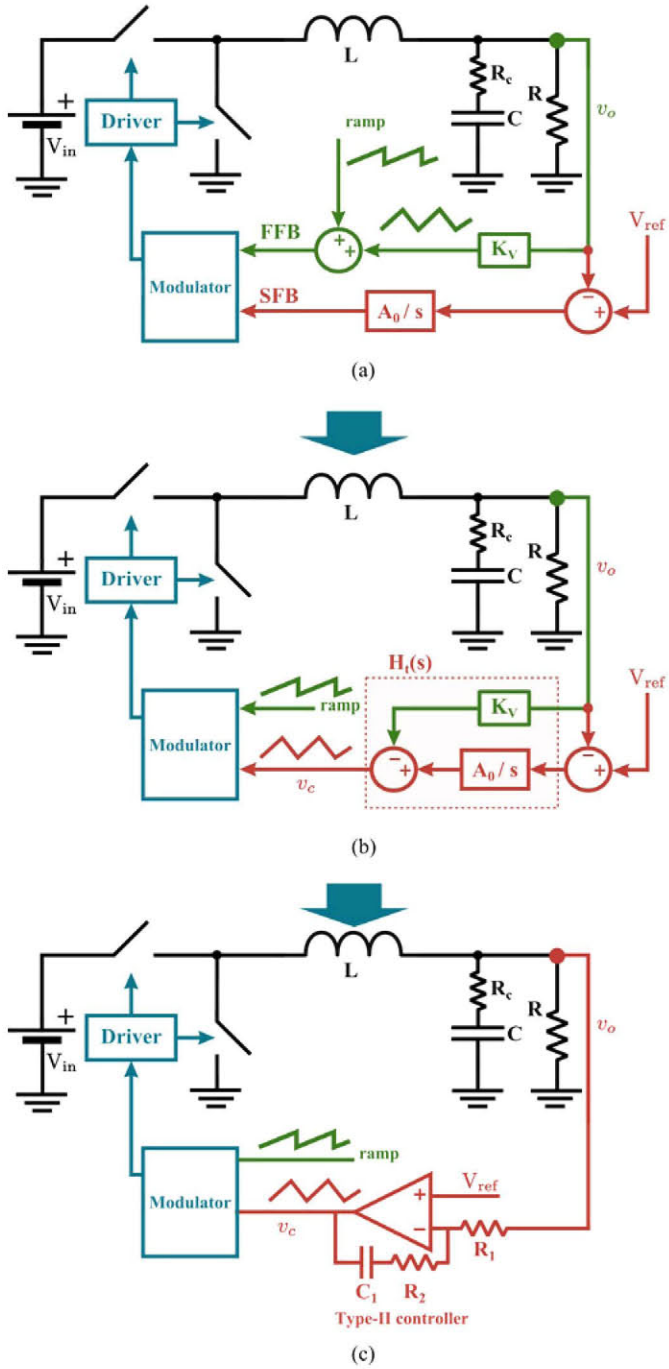

Fig. 19. Implementation of a v^2 control as a conventional type-II controller.

$$H_t(s) = A_0/s + K_v. \tag{18}$$

Fig. 20 shows the equivalent compensator of v^2 control modulated with constant on-time for the same case as Fig. 1. The power stage has the following parameters: $V_{\text{in}} = 5$ V, $v_o = 1.2$ V, $L = 1.3\ \mu$H, $C = 300\ \mu$F, $R_c = 13\ \text{m}\Omega$, $T_{\text{on}} = 670$ ns. The control parameters of v^2 are [see Fig. 19(a)] $K_v = 2$, $A_0 = 5000$. The compensating ramp is eliminated. The resulting

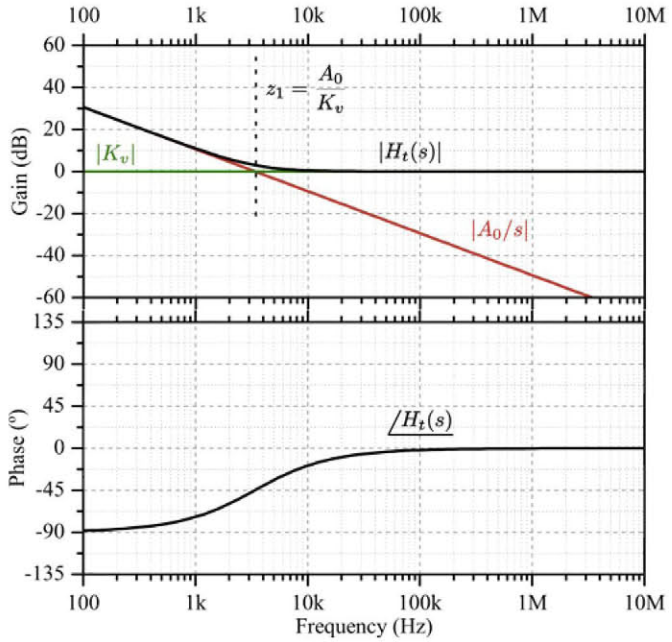

Fig. 20. Type-II controller for an output capacitor with ESR-zero at low frequencies.

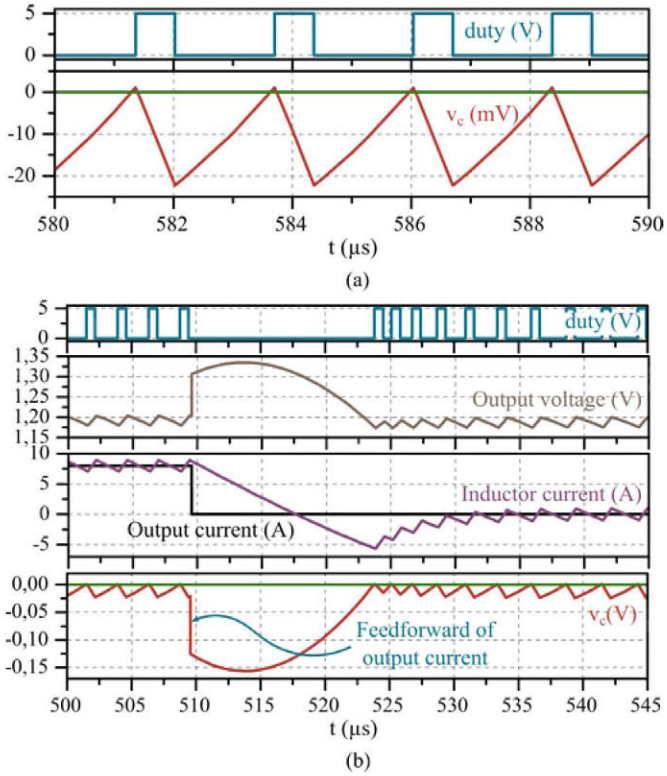

Fig. 21. Large-signal behavior of the type-II voltage-mode control with constant on-time modulation for an output capacitor with ESR-zero at low frequencies. (a) Steady-state signals of the comparator. (b) Load transient response 8 A→ 0 A.

exact passive elements of the type-II voltage mode are [see Fig. 19(c)] $R_1 = 1$ kΩ, $R_2 = 2$ kΩ, $C_1 = 200$ nF.

Fig. 21 shows the large-signal behavior of the designed type-II voltage-mode control. Fig. 21(a) shows the steady-state behavior of the signals of the comparator v_c and zero for this case without the ramp. Note that the voltage-mode control can be modulated without ramp and with constant on-time. Fig. 21(b) shows the load transient response under a load step 8 A → 0 A. Comparing with the v^2 control of Fig. 1(b), that is designed with the same parameters, the dynamic response is the same. The response is near time optimal and exhibits a feedforward of the output current because the ripple of the ESR of the output capacitor is dominant in the output voltage. Consequently, it has been shown that the v^2 control is equivalent to a type-II voltage-mode control.

V. Design Considerations of the Proposed Voltage-Mode Control Based on the v^1 Concept

As stated, the controls based on the v^1 concept behave like a current-mode control. Of course, this does not mean that they can be used to ensure current sharing in parallel converters, but that these controls use the current information of the output voltage. As opposed to traditional designs of voltage-mode controls, the regulator of these controls does not act as a low-pass filter, since high-frequency information is allowed to go through. By doing this, as seen in Section IV, a very fast transient response can be obtained. The downside is that the control is prone to subharmonic oscillations because side-band frequencies are not attenuated by the controller and are fed back to the modulation stage. In order to better explain this occurrence, Fig. 22 shows the representation of the harmonic content of the control signals

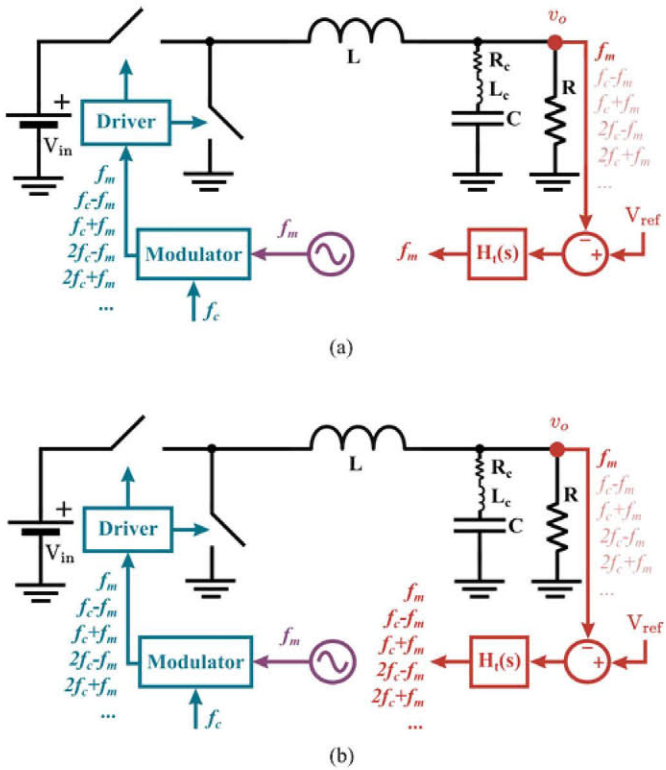

Fig. 22. Representation of harmonic content for two different designs of voltage-mode control. (a) Traditional design of voltage-mode control. (b) Proposed design of voltage-mode control.

of a traditional design and the proposed design based on the v^1 concept of a voltage-mode control.

(1) Fig. 22(a) shows the representation of the harmonic content of the control signals of a common design of a voltage-mode control. When the modulator is perturbed with a sine of modulation frequency f_m, the modulator produces side-band frequencies, besides the modulation frequency [34]–[36]. These side-band frequencies are $f_c \pm f_m$, $2f_c \pm f_m$, etc., where f_c is the carrier frequency of the modulator. Then, the output voltage has a harmonic content that is mostly dominated by the modulation frequency because the side-band frequencies are attenuated by the *L*–*C* filter of the power stage that acts as a low-pass filter. Additionally, the controller of the voltage-mode control is normally designed as a low-pass filter that attenuates even more the side-band frequencies. As a consequence, for practical purposes, the control returns to the modulator a signal with a frequency content of the modulation frequency.

(2) On the other hand, Fig. 22(b) shows the representation of the harmonic content of the control signals of the proposed design of a voltage-mode control using the v^1 concept. Now, because the current information of the output voltage is effectively used in the control, the controller is designed to, not only let the side-band frequencies pass, but increase them instead of attenuating them. As a result, the side-band frequencies are fed back to the modulator, which is the origin of the subharmonic oscillations in current-mode controls.

As seen, in traditional designs of voltage-mode control, there is no problem with subharmonic oscillations. But in the proposed designs of voltage-mode control there is, just as in current-mode control. Furthermore, the designs require the poles of the controller to match the zeros of the impedance of the output capacitor so deviations from the exact values might move the control closer to instability. Consequently, a careful design of the control is needed.

Fig. 23 shows the design flow of a systematic way to design the proposed voltage-mode control based on the v^1 concept. The idea is to first calculate the values A_0, K_v, and K_i of its implementation as a $v^2 i_c$ control, which can always implement the exact controller of (1). The modeling and equivalent circuits based on the Describing function [37], [38] can be used to provide physical insight and an initial design. In [11], a design guideline for the gain of the capacitor current K_i is proposed for constant on-time modulation. Then, a more accurate analysis is needed to account for tolerances of the parameters and mismatches of the current sensor. In [31], a methodology that takes into account all the above is proposed to evaluate the stability of converters based on discrete modeling and Floquet theory. With these tools, an optimization algorithm can be created that designs the controls to behave very fast, while assuring robustness under the whole operation region, accounting for tolerances of parameters and sensing networks [32]. Additionally, a commercial simulation program that can work with switched-mode power supplies and frequency responses is a good supplementary tool to design the $v^2 i_c$ control. Once the three parameters of

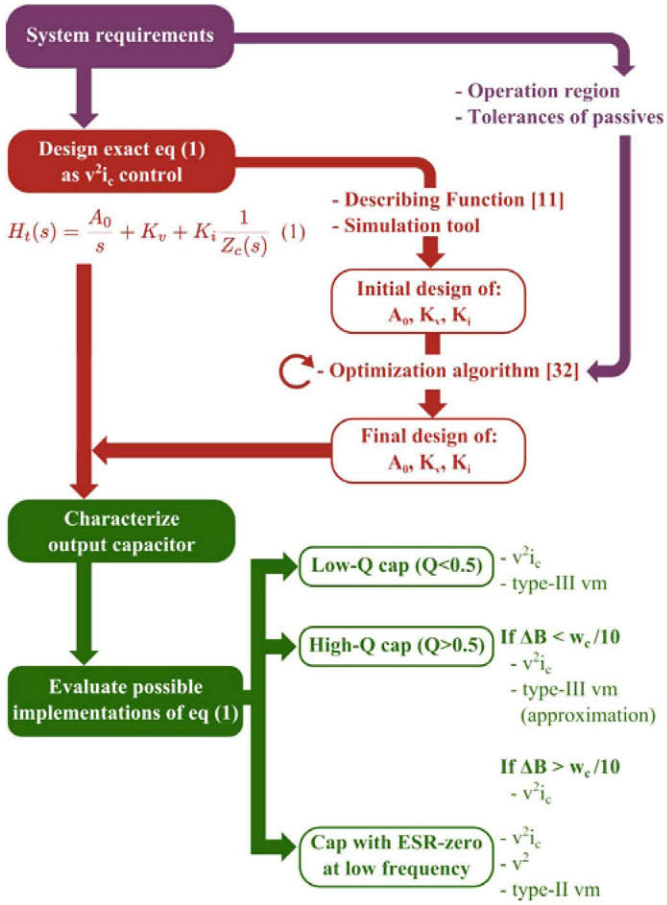

Fig. 23. Design flow of the proposed voltage-mode control based on v^1 concept.

the control A_0, K_v, and K_i are calculated, its implementation as a traditional voltage-mode control can be considered according to Section IV. Recall that, for low-Q output capacitors, the robustness and dynamic response of the voltage-mode control is the same as the $v^2 i_c$ control. For high-Q output capacitors, the robustness depends on the position of the resonant frequency of the capacitor with respect to the bandwidth of the control.

VI. Experimental Validation

This section validates the design of the type-III voltage-mode control of Section IV-B for the case of high-Q output capacitor, where its impedance has a resonance produced by the C and the ESL, and compares to its implementation as a $v^2 i_c$ control. This case is chosen to validate the proposed design methodology because it is the worst case, since an approximation is required and an experimental validation is therefore needed. Remember that, for the case of a high-Q output capacitor, a type-III voltage-mode control can be designed with the same response as $v^2 i_c$ only if the bandwidth of the loop gain is at least one decade below the resonance frequency of the output capacitor. The parameters of the power stage and the controls are the same as in Section IV-B. Both controls are perturbed with a load step from 8 to 0 A. The load step is placed at the beginning of the on-time on purpose

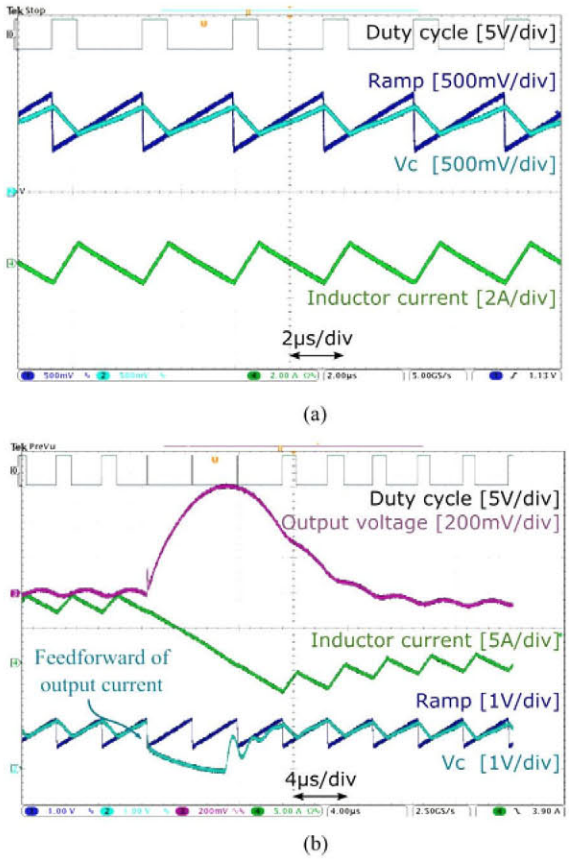

Fig. 24. Experimental validation of large-signal behavior of $v^2 i_c$ control. (a) Steady-state signals of the comparator. (b) Load transient response 8 A $\rightarrow$ 0 A.

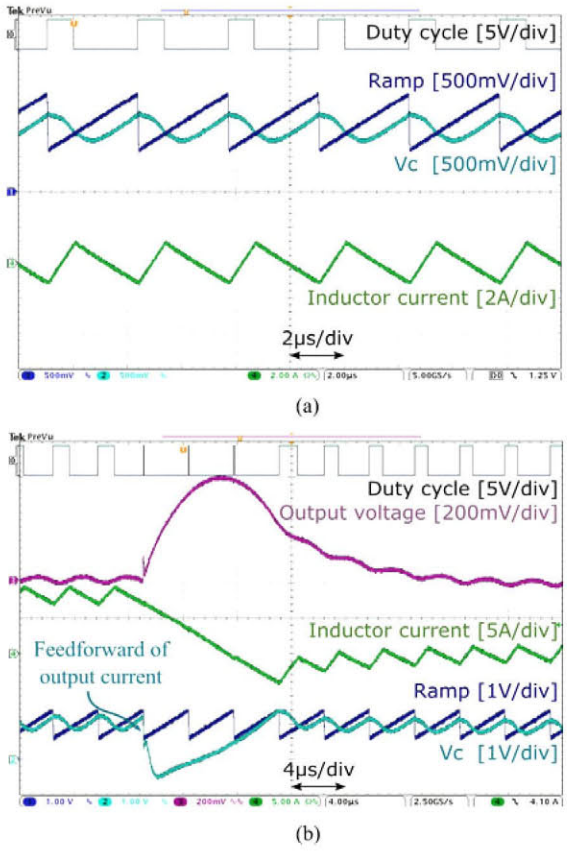

Fig. 25. Experimental validation of large-signal behavior of proposed design of type-III voltage-mode control. (a) Steady-state signals of the comparator. (b) Load transient response 8 A $\rightarrow$ 0 A.

because, in order to react optimally, an extremely fast reaction is needed to command an on-time as small as possible. Fig. 24(a) shows the steady-state behavior and the dynamic response of the $v^2 i_c$ control reordered as in Fig. 6. Note that the results are very similar to Fig. 16. Fig. 25(a) shows the steady-state behavior and the dynamic response of the type-III voltage-mode control. Note again that the results are very similar to Fig. 17 and that the control exhibits a feedforward of the output current. This behavior that mirrors the output current in the output voltage is because the control is designed according to (1) and Fig. 7 and it is what allows a very fast reaction just after the load transient. Consequently, it has been shown in an experimental prototype that both $v^2 i_c$ and a type-III voltage-mode control can achieve the same transient response.

Fig. 26 shows the comparison of the measured regulators $H_t(s)$ and loop gains $L(s)$ of $v^2 i_c$ and a type-III voltage-mode control. The Bode 100 analyzer is used to perform the measurements. Note that it is very similar to Fig. 15 and that the equivalent regulator of $v^2 i_c$ exhibits complex poles as predicted. The position of the second zero and the real poles of the type-III voltage-mode control does not match exactly the equivalent regulator of $v^2 i_c$ control because, in the implementation, it is needed to modify slightly the resistances and capacitances of the linear controller to use commercial values. Specifically, in the prototype, the actual values are $R_1 = 7.87$ kΩ, $R_2 = 1.6$ kΩ,

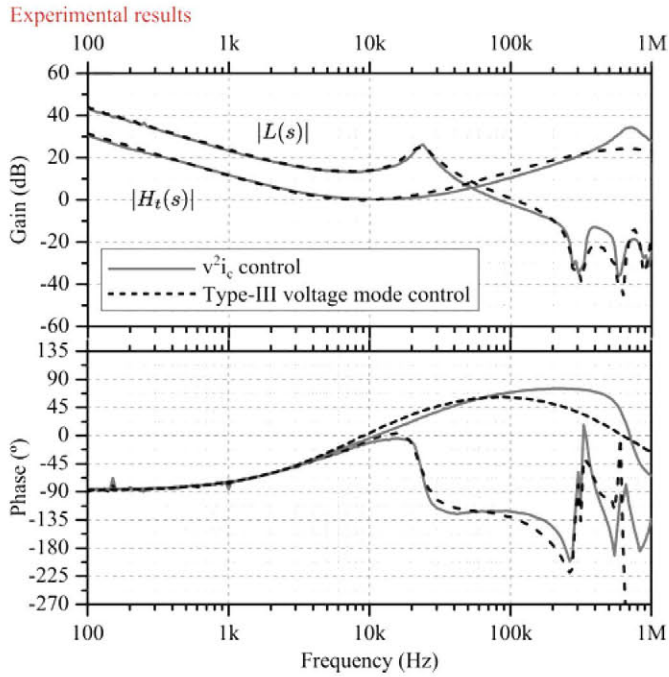

Fig. 26. Comparison of the measured regulators $H_t(s)$ and loop gains $L(s)$ of $v^2 i_c$ and the proposed design of type-III voltage-mode control.

$R_3 = 47\ \Omega$, $C_1 = 150$ pF, $C_2 = 5.6$ nF, $C_3 = 4.7$ nF. However, the transient responses of both controls are almost exactly the same, so there is no need for a perfect matching of the poles and zeros.

VII. Summary and Conclusion

This paper has proven both in simulation and in an experimental prototype that sensing the output voltage is all that is needed to react almost optimally under a load transient. This is because, in a buck converter, the output voltage has information about almost all the signals of the power stage. This property is what we call the v^1 concept. By exploiting this feature, a traditional voltage mode can be designed to behave as a current-mode control and to achieve a near time-optimal load transient response. This does not mean that the control can be used for current sharing but that the current information hidden in the output voltage is effectively used to react very fast. The basic idea to achieve this is that, at high frequencies, the regulator needs to behave as the inverse of the impedance of the output capacitor. This way, the voltage information is converted to current information and, then, the voltage loop has information about the capacitor current and, consequently, about the output current. This provides the control, a kind of a feedforward of the output current by only sensing the output voltage.

This paper has analyzed for different quality factors Q of the output capacitor, the possible different implementations of the control sensing only the output voltage.

1) For low-Q output capacitors with the ESR effect above the bandwidth, the control can be implemented either as a $v^2 i_c$ or alternatively as a type-III voltage-mode control.
2) For high-Q output capacitors so that the C and the ESL create two conjugate complex zeros, the control can always be implemented as a $v^2 i_c$. If the bandwidth of the control is at least one decade lower than the resonant frequency of the output capacitor, then the control can implemented also as a the type-III voltage mode. Otherwise, $v^2 i_c$ is the only possible implementation.
3) For low-Q output capacitors with the ESR effect below the bandwidth, the control can be implemented as a v^2, $v^2 i_c$, or alternatively as a type-II voltage-mode control.

Additionally, design considerations are given. As a consequence of the proposed design using the v^1 concept, the controller does not attenuate the side-band frequencies produced by the modulator. As a result, the control is prone to subharmonic oscillations as in a current-mode control. This paper proposes a design flow based on the calculation of the parameters of the $v^2 i_c$ control with the available methods from the literature and, then, consider its implementation as a traditional voltage-mode control.

With all this information, low cost very fast controllers that only sense the output voltage can be designed and manufactured.

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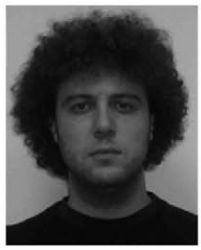

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